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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,706	10/14/2003	Kimble Dong	38493-8006US1	4838

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EXAMINER	
HENDERSON, ADAM	
ART UNIT	**PAPER NUMBER**
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/684,706	DONG, KIMBLE	
	Examiner	Art Unit	
	Adam L. Henderson	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Regarding claim 7, the phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 7, 8, 11, 12, 14, 18, 21, 23, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Younse et al. (US Patent 4,805,023).

6. With regard to claim 1 Younse et al. disclose a MOS image sensor comprising [since the MOS statement is in the preamble and nothing within the body further requires that the sensor be of MOS type, the limitation in the preamble is not given patentable weight]:

a pixel array formed from a plurality of pixels arranged in a matrix of rows and columns (FIG. 1, CCD);

location processing means for providing a digital location number for each pixel of the pixel array (column 2 lines 46-55);

signal processing circuitry for reading out signals from the pixel array and outputting processed pixel signals (column 2 lines 43-68);

dead pixel comparator circuitry for receiving the processed pixel signals from the signal processing circuitry and examining the processed pixel signals to see if they are indicative of dead pixels (column 2 lines 52-68);

location storage circuitry for receiving dead pixel information from the dead pixel comparator circuitry and for storing the digital location number generated by the location processing means for each dead pixel (column 2 lines 62-68); and

location comparator circuitry for comparing the digital location number of a pixel that is being processed by the signal processing circuitry with the stored digital location numbers of dead pixels to determine if the pixel that is being processed corresponds to a dead pixel (column 3 lines 1-30).

7. With regard to claim 2 Younse et al. disclose the image sensor of claim 1, wherein the location processing means comprises a location shift register for indicating the digital location number of each of the pixels to the pixel array, the location comparator circuitry, and the location storage circuitry (pixel address counter, column 3 lines 1-30).

8. With regard to claim 7 Younse et al. disclose the image sensor of claim 1, wherein the location storage circuitry is coupled to an off chip storage area (PROM, FIG. 2, column 2 lines

43-68) such as an EPROM ["such as an EPROM" is vague and indefinite and therefore is not being considered since it is not clear whether the storage area can only be an EPROM].

9. With regard to claim 8 Younse et al. disclose a method for correcting for dead pixels in a MOS imaging array, said imaging array including a plurality of pixels arranged in a matrix of rows and columns [since the MOS statement is in the preamble and nothing within the body further requires that the sensor be of MOS type, the limitation in the preamble is not given patentable weight], said method comprising the steps of:

sequentially examining the signals from each pixel in the imaging array to determine if each pixel is a dead pixel (column 2 lines 43-68);

storing a location number of each dead pixel (column 2 lines 43-68);

after all of the dead pixels have been determined and their location numbers stored, proceeding with normal image processing of the imaging array, during which as the signal from each pixel is read out, the location number of each pixel is compared with the stored location numbers for dead pixels, and the signal from any pixel with a location number that corresponds to the stored location number of a dead pixel is compensated for (column 3 lines 1-30).

10. With regard to claim 11 Younse et al. disclose the method of claim 8, wherein the location numbers of the pixels are produced by a location shift register (pixel address counter, column 3 lines 1-30).

11. With regard to claim 12 Younse et al. disclose the method of claim 8, wherein a location comparator is used to perform the step of comparing the location number of a pixel with a stored location number for a dead pixel (column 3 lines 1-30).

12. With regard to claim 14 Younse et al. disclose A method for correcting for dead pixels in a MOS imaging array, said imaging array including a plurality of pixels arranged in a matrix of rows and columns [since the MOS statement is in the preamble and nothing within the body further requires that the sensor be of MOS type, the limitation in the preamble is not given patentable weight], said method comprising the steps of:

(a) reading out a pixel signal from a pixel in the pixel array (column 2 lines 43-68);

(b) determining if the pixel signal from the pixel indicates that the pixel is a dead pixel (column 2 lines 43-68);

(c) storing a location number of a dead pixel (column 2 lines 43-68);

(d) repeating steps (a) to (c) for each pixel in the pixel array until all of the pixels have been read out (column 2 lines 43-68); and

(e) thereafter comparing the location number of each pixel that is being read out with the stored location numbers of dead pixels and compensating for the signal from a pixel whose location number corresponds to the stored location number of a dead pixel (column 3 lines 1-30).

13. With regard to claim 18 Younse et al. disclose A method for correcting for dead pixels in a MOS imaging array, said imaging array including a plurality of pixels arranged in a matrix of rows and columns [since the MOS statement is in the preamble and nothing within the body further requires that the sensor be of MOS type, the limitation in the preamble is not given patentable weight], said method comprising the steps of:

(a) generating a location number for a pixel in the pixel array and reading out the signal from the pixel (column 2 lines 43-68);

(b) determining if the signal from the pixel indicates that the pixel is a dead pixel (column 2 lines 43-68);

(c) if the signal from the pixel indicates that the pixel is a dead pixel, storing the location number of the dead pixel in a storage area (column 2 lines 43-68);

(d) repeating steps (a) to (c) until all of the pixels have been read out (column 2 lines 43-68);

(e) after all of the pixels have initially been read out and the dead pixel location numbers have been stored, reading out a signal from a pixel in the pixel array (column 3 lines 1-30);

(f) comparing the location number of the pixel that is currently being read with the stored location numbers of the dead pixels (column 3 lines 1-30);

(g) compensating for a pixel whose location number corresponds to a stored location number of a dead pixel (column 3 lines 1-30); and

(h) repeating steps (e) to (g) for all of the pixels in the pixel array to produce each frame of the image signal (column 3 lines 1-30).

14. With regard to claim 21 Younse et al. disclose an image sensor comprising:

a pixel array formed from a plurality of pixels arranged in a matrix of rows and columns (CCD, FIG. 1);

signal processing circuitry for reading out signals from the pixel array and outputting processed pixel signals (column 2 lines 43-68);

a location shift register for incrementing location numbers for pixels in the pixel array (pixel address counter, column 2 lines 43-68); and

dead pixel comparator circuitry for receiving the processed pixel signals from the signal processing circuitry and examining the processed pixel signals to see if they are indicative of dead pixels, and for indicating when the location number of a pixel that is determined to be a dead pixel should be stored (column 2 lines 43-68).

15. With regard to claim 23 Younse et al. disclose the image sensor of claim 21, further comprising location storage circuitry for storing the location numbers of dead pixels (PROM, FIG. 2, column 2 lines 43-68).

16. With regard to claim 24 Younse et al. disclose the image sensor of claim 23, further comprising location comparator circuitry for comparing the location number of a pixel that is being processed by the signal processing circuitry with the stored location numbers of dead pixels from the location storage circuitry to determine if the pixel that is being processed corresponds to a dead pixel (column3 lines 1-30).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 3, 4, 9, 10, 15, 16, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Younse et al. (US Patent 4,805,023) in view of Lin et al. (US Patent 4,920,428).

19. With regard to claim 3 Younse et al. disclose the image sensor of claim 1, but fail to disclose wherein the signal processing circuitry compensates for a dead pixel by repeating a pixel signal from a pixel that was read out prior to the dead pixel.

Lin et al. disclose wherein the signal processing circuitry compensates for a dead pixel by repeating a pixel signal from a pixel that was read out prior to the dead pixel (column 5 lines 65-68).

It would have been obvious at the time of the invention to one skilled in the art to combine the image sensor of Younse et al. to include the replacement technique of Lin et al. in order to provide an alternative replacement method hat is well known.

20. With regard to claim 4 Younse et al. disclose the image sensor of claim 1, but fail to disclose wherein the signal processing circuitry compensates for a dead pixel by averaging the pixel signal from a pixel that was read out prior to the dead pixel with a pixel signal from a pixel that is read out subsequent to the dead pixel.

Lin et al. disclose wherein the signal processing circuitry compensates for a dead pixel by averaging the pixel signal from a pixel that was read out prior to the dead pixel with a pixel signal from a pixel that is read out subsequent to the dead pixel (column 6 lines 1-2).

It would have been obvious at the time of the invention to one of ordinary skill in the art to combine the image sensor of Younse et al. to include the replacement technique of Lin et al. in order to provide an alternative replacement method hat is well known.

21. All limitations contained in claims 9, 10, 15, 16, 19 and 20 are addressed in the rejections of claims 3 and 4. Claims 9, 10, 15, 16, 19 and 20 are therefore likewise rejected.

22. Claims 5, 6, 13, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Younse et al. (US Patent 4,805,023) in view of Katoh et al. (US Patent 5,796,430).

23. With regard to claim 5 Younse et al. disclose the image sensor of claim 1, but fail to disclose wherein the dead pixel comparator is initially activated when the image sensor is first powered on to examine the processed pixel signals from each pixel only once.

Katoh et al. disclose wherein the dead pixel comparator is initially activated when the image sensor is first powered on to examine the processed pixel signals from each pixel only once (column 3 line 50 – column 4 line 54).

It would have been obvious at the time of the invention to one of ordinary skill in the art to combine the image sensor of Younse et al. with the power-on examination taught by Katoh et al. in order improve the detection ability by setting a regular reexamination point. This would sure that the system would regularly check for any new pixels that had died.

24. With regard to claim 6 Younse et al. disclose the image sensor of claim 5, but fail to disclose wherein the dead pixel comparator may be activated at later times to reexamine the processed pixel signals from each pixel so as to update the dead pixel digital location numbers stored in the location storage circuitry.

Katoh et al. disclose wherein the dead pixel comparator may be activated at later times to reexamine the processed pixel signals from each pixel so as to update the dead pixel digital location numbers stored in the location storage circuitry (column 6 lines 23-41) [turning the system off may also activate the detection process].

It would have been obvious at the time of the invention to one of ordinary skill in the art to combine the image sensor of Younse et al. with the power-on examination taught by Katoh et

al. in order improve the detection ability by setting a regular reexamination point. This would sure that the system would regularly check for any new pixels that had died.

25. All limitations contained in claims 13 and 17 are addressed in the rejections of claims 5 and 6. Claims 13 and 17 are therefore likewise rejected.

26. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Younse et al. (US Patent 4,805,023) in view of Ackland et al. ("Camera on a Chip").

27. With regard to claim 22 Younse et al. discloses the image sensor of claim 21, but fails to disclose wherein all of the circuitry of the image sensor is fabricated on a single MOS chip.

Ackland et al. disclose wherein all of the circuitry of the image sensor is fabricated on a single MOS chip (FIGS. 1 and 2, page 24 column 1 first full paragraph on the page) [Ackland shows that all the components of a CCD camera that are spread across several chips may be combined into a single CMOS manufactured chip using a CMOS sensor instead of a CCD sensor].

It would have been obvious at the time of the invention to one of ordinary skill in the art to combine the image sensor of Younse et al. with the single MOS chip of Ackland et al. in order to lower the cost of the completed parts (Ackland et al, page 25 column1 last paragraph).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adam L. Henderson whose telephone number is 571-272-8619. The examiner can normally be reached on Monday-Friday, 7am to 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ALH
5 January 2007

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER